INTEGRATED ASW SYSTEM STUDY

By

George K. Kostopoulos

January 1973

INTEGRATED ASW SYSTEM

STUDY

Introduction

A. Evaluation of Fast Fourier Transform Processors

B. Selection of Digital Signal Processing Hardware

C. Trade-Off Between Software and Hardware in Digital Signal Processing

D. Front-End Multiplexing

E. Real-Time Multi-Port Controllers

Summary

Introduction

A study was conducted on all major commercially available digital signal processing systems, where each one was evaluated for use in acoustic-sonar environment.

The results of this study, along with current knowledge on the Navy's requirements in the area of digital signal processing, served as a background for the development of guidelines for the following items:

A. Evaluation of Fast Fourier Transform (FFT) Processors

B. Selection of digital signal processing hardware

C. Trade-off between software and hardware in digital signal processing

In addition to the above items, design approaches were considered for

D. Front-end multiplexing, and

E. Real-time multi-port controllers

A. Evaluation of Fast Fourier Transform (FFT) Processors

Sonar signal analysis offers a large amount of information which reveals important characteristics about the environment of the underwater signal and about its source in the case of passive detection. The key to reliable identification of these characteristics is refined analysis.

The primary factors that contribute to a refined analysis are:

1. Digital resolution of input signal
2. Size of trigonometric coefficient
3. Number of spectral lines produced by the analysis, and
4. Speed

The digital resolution of the input signal is determined by the number of bits of the analog to digital converter used for the conversion of the input signal, and directly affects the dynamic range of the front end of the signal processing system. It is the high dynamic range that will retrieve weak signals riding over strong ones or noise. The bits to db relationship is about 6 db per bit. Today's signal analysis needs require a minimum of 12 bits of analog to digital conversion (65 db), with 16 bits (90 db) being a more typical requirement.

The size (number of bits) of the trigonometric coefficients that are multiplied by the sampled values of the input signal in the FFT process should equal or exceed the size of the sampled signal. In order to maximize the resolution that results from the FFT process, the multiplactions performed in that process should extend to about twice the number of bits of the input signal. The final results of the FFT computation, which represent the

spectrum amplitude may, of course, be truncated to a small number of bits sufficient for a meaningful spectral display.

Equally significant to amplitude resolution is frequency resolution. This is represented by the number of spectral lines produced by the FFT process. Present systems offer variable frequency resolution typically ranging from 64 to 4096 spectral lines per bandwidth. The upper limit of this range is restricted by the memory size allotted for the FFT array computations and not by the arithmetic unit of the processor. Today's demands for precise underwater environment definition requires spectra to be represented by at least 2048 spectral lines. Twice that much should be the guideline in the evaluation of FFT systems operational beyond the '70's.

The speed in which an FFT process is performed is of considerable significance because it determines the maximum frequency that can be analyzed as well as the number of channels that can share a single FFT processor. Present systems offer 512 spectral lines in about 16 ms, while the projected needs for beyond the '70s are 4096 spectral lines in the same time length. Single FFT processor performance does not, presently, meet these future requirements. Eventually, however, when the "butterfly operation" of the FFT process is produced in high speed LSI form the above requirements will be met.

The secondary factors that contribute to a refined signal spectrum analysis are:

1. Hanning ability
2. Redundancy
3. Zoom analysis

4. Averaging
5. Inverse transform

Other desirable features that add flexibility to a signal processing system are:

Auto spectrum

Auto correlation

Cross spectrum

Cross correlation

Transfer function

Coherence function

B. Selection of Digital Signal Processing Hardware

The hardware selection of a digital signal processing system is based on the technical evaluation described in the preceding section and on factors defined as system criteria, related to the specific application.

The major system criteria are:

1. System expandability
2. Signal processor interaction with remaining system (central computer, peripherals, display), and
3. Storage capability

A digital signal processing system must be expandable in terms of input channels and output display equipment to accommodate future additions to the system. Pipeline FFT operations often prevent high speed multiplexing of the processor, thus limiting channel expandability.

Interface and simple interaction between signal processor and remaining system is the key to reliable operation. FFT processor should be easily interfaced to the data bus of the remaining system and should preferably employ the same type of computer as the overall system does. This way consistency in programming will exist throughout the system. Initiation of performance of functions should require the minimum of input from the operator, preferably a simple code sent through the control keyboard or the depression of a button at the processor's panel.

Storage capability in the FFT processor directly affects performance expandability. Therefore, ample storage for array manipulation is necessary, especially when off-line functions are performed (correlations, coherence, etc.).

Other factors that influence hardware selection is system compactness and maintainability.

When the FFT processor is part of a larger system, the processor's physical size can be very critical, especially in airborne and underwater applications, and FFT processor size determination should include the FFT arithmetic unit as well as its memory and control equipment.

Because of their increasing complexity, FFT systems require frequent preventive maintenance. Therefore, thorough supporting software for testing and troubleshooting should accompany every eligible system.

C. Trade-Off Between Software and Hardware in Digital Signal Processing

The FFT process mainly consists of "butterfly operations" and of data transfers. Because of their complexity resulting in excessive time consumption, "butterfly operations" should be performed by high speed hardware while data transfers can be executed by the software.

Hanning weighting function should be preferably hardwired, thus saving about 5 percent of processing time.

There is considerable room for software -- hardware tradeoff in the design of interface controllers for the mass storage devices. Every effort put into the controllers design to relieve software always simplifies system overall operation, in addition to increasing processing speed. This is especially applicable to block data transfers.

Another area of hardware over software preference is front-end multiplexing. Because of their complexity and asynchronous repetition, front-end multiplexing should be mainly executed by hardware.

On the other hand, areas where the software should dominate are post-FFT processing and display formatting, since these operations change depending on the viewpoint of the application and analysis.

D. Front-End Multiplexing

In a real-time multichannel signal processing operation, multiplexing of the FFT processor requires special attention. It is important that no data be lost and that the FFT processor be working to its full capacity whenever so needed.

Because of the continuous availability of new data, temporary storage provisions are required that will enable data storage in block form and subsequent transfer of these data to the FFT processor.

To facilitate data transfers, temporary storage must be integrated into the front-end multiplexing configuration. In a multichannel operation, new data are generated by the input channels independently of the FFT processor timing. Consequently, the A-D conversion and the temporary storage of data need not be supervised by any computer routine.

Instead, the front-end multiplexing unit will be notifying the FFT processor at the end of each data block. Data blocks should correspond to data frames.

Figure 1 illustrates an approach to multiplexing 20 channels of sonar signals into one data channel.

The A-D converter accepts 20 filtered analog signals and provides their digital equivalent to 8 bits with negative values represented in 2's complement.

The 20 channels are simultaneously sampled. The samples are stored in analog form and are sequentially converted to serial digital form.

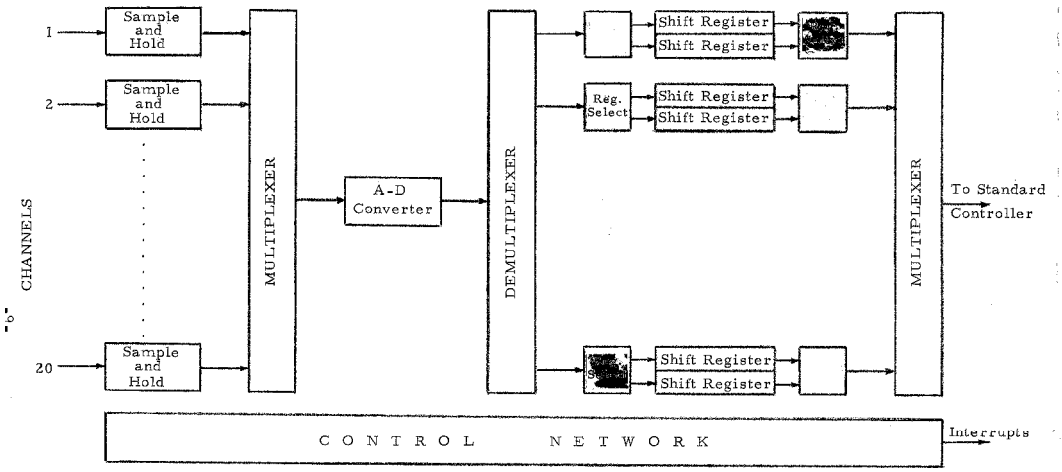

FIGURE 1. FRONT-END MULTIPLEXING UNIT

The method of "successive approximation" is most suitable for the A-D conversion since it is fast and provides the digital output in serial form as well as in parallel form.

The A-D converter clock frequency is calculated as follows:

Sampling Rate = 2 (Bandwidth) $\quad BW_{max} = 2500\,Hz$
= 2 (2500)
= 5 kHz

A-D Converter Clock Frequency = (Number of Bits) x (Sampling Rate)
= 8 x 5 kHz
= 40 kHz

If the one A-D converter is used for all 20 channels, its minimum clock frequency should be

A-D Converter Clock Frequency = (Number of Channels). (Number of Bits). (Sampling Rate)
= 20 x 8 x 5 kHz
= 800 kHz

If channels are not sampled simultaneously, the maximum time shift between channels will be

Time Shift = (Number of Bits)·(Number of Channels -1)·(Clock Period)
= 8 x (20 - 1)/800 kHz
= 190 microseconds

If the clock frequency is increased, the time shift may be brought below maximum limit, thus eliminating the need for the sample and hold circuitry.

The output of the analog to digital converter is demultiplexed and stored into 8 x N-bit shift registers, where N is the number of points per frame.

There are two sets of twenty shift registers per channel. One of the two sets accepts data from the analog to digital converter, while the other transfers data to the FFT processor via DMA. The role of the two shift register sets interchanges at the end of each data frame. Thus, the shift registers accept data from the demultiplexer at the A-D converter's rate and transfer that data to the FFT processor at the processor's rate.

This transfer is under FFT processor software control, preferably initiated by means of an interrupt, where the interrupt is generated by the control circuit of the multiplexing unit at the end of each frame A-D conversion.

E. Real-Time Multi-port Controllers

To determine the relationship between mass storage and the manner in which a real-time multi-port controller would be structured, a multi-port disc controller was designed, and it is illustrated in Figure 2.

The controller's function was to interface the disc with eight data channels as well as with the system's computer.

As in the case of front-end multiplexing, intermediate storage of input data is the primary consideration. The form of storage should be such that it accommodates two data rates; that of the external devices and that of the mass memory system.

Since the magnetic disc stores information in serial form, intermediate storage devices of similar characteristics should be employed. Shift registers fall in this category and should be used as a buffer between the data producing device and the disc.

Data may enter a shift register at one rate and exit at another, thus accommodating the data rate difference between data generating devices and storage disc.

Another consideration related to multiport interfacing is need for individual interrupt, or sense, lines. These lines will notify the computer that data are available for transfer from intermediate storage to either the computer or to the disc.

Adequate software provisions should exist in order to easily facilitate supervision of the multiport data traffic.

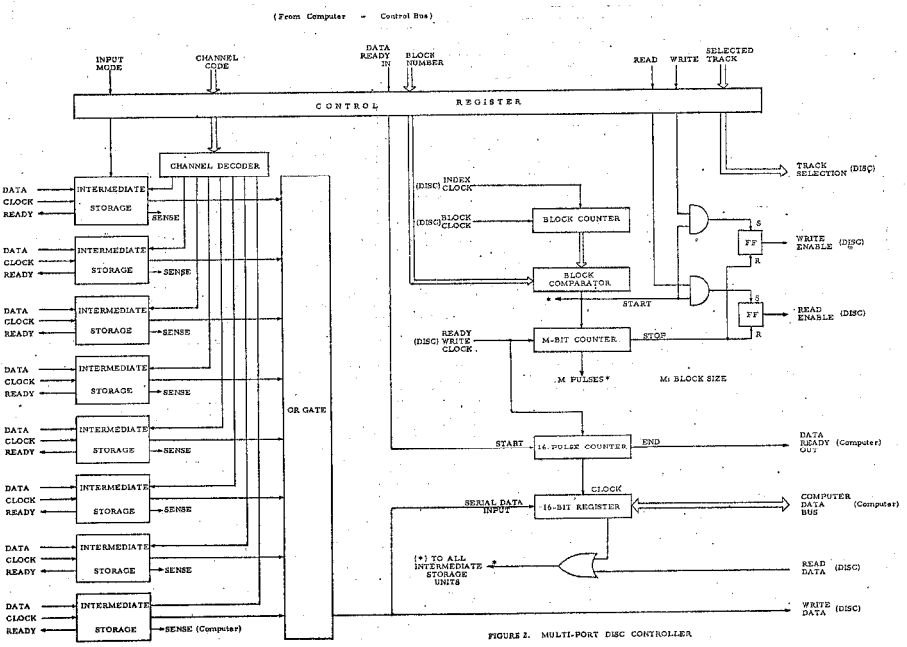

FIGURE 2. MULTI-PORT DISC CONTROLLER

The above considerations apply to multi-port interfacing in general. Additional specific considerations shall arise once specific hardware are evaluated.

SUMMARY

The conducted study has resulted in an extensive familiarity with the FFT process and its application to underwater acoustics, and into the development of guidelines for the evaluation and selection of FFT equipment.

The selection of a suitable FFT processor and its integration into the present computer/display system can be the follow-up to this study. Such task will make considerable utilization of our Laboratory's EDP potentials and open up new study contract horizons.