IDEAS FOR DESIGN

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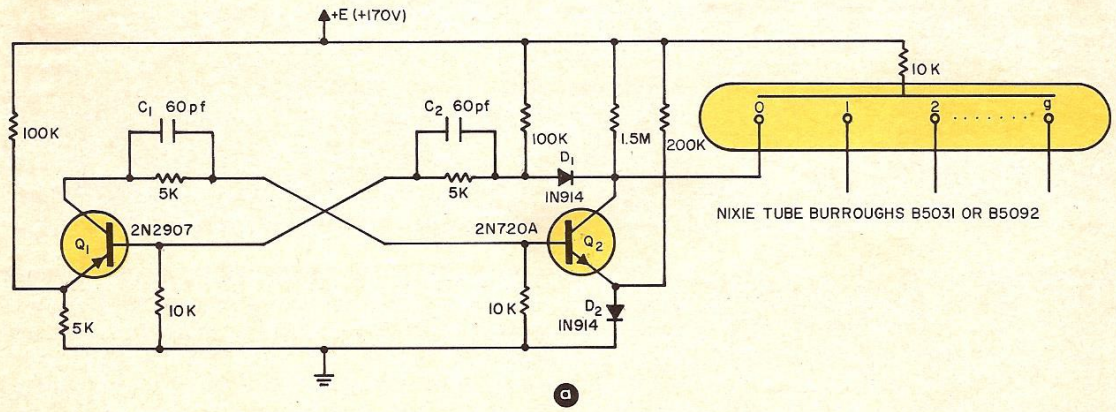
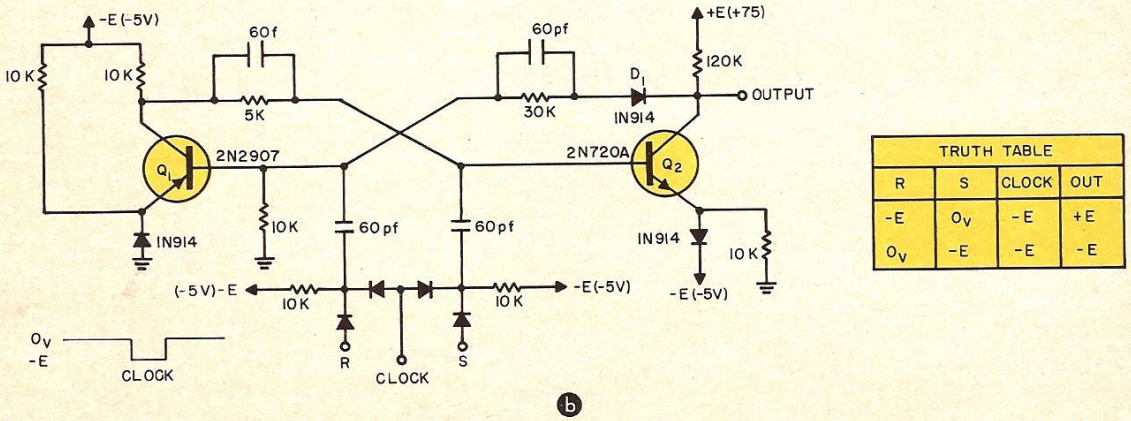
Nixie driver flip-flop also stores information

In many applications, Nixie tube drivers are controlled by flip-flops. The flip-flops are employed to keep the driver of the Nixies at the desired state until new information (from additional circuitry) is received. It would be desirable to have one circuit perform two functions—driving of the Nixies and storing of the information.

The pnp-npn flip-flop shown in Fig. 1a stores and drives simultaneously and has very-low power dissipation. Each of the 10 cathodes of the Nixie can be connected to this circuit.

Both transistors are either ON or OFF. When they are ON, Q_2's collector is at a low negative potential. This allows the Q_1 base current to flow, thus keeping it ON. Q_1's collector is then at a sufficient negative potential to keep Q_2 ON. At this stage, V_{out}





TRUTH TABLE			
R	S	CLOCK	OUT
-E	O_V	-E	+E
O_V	-E	-E	-E

1. **Complementary flip-flop arrangement** stores information and drives Nixie tubes (a). Modification of this circuit (b) results in closed R-S flip-flop operation.

is approximately +1 volt, and the Nixie is ON. This state can be initiated by a positive pulse at C_4.

When they are OFF, Q_1 is reverse biased by the voltage divider action of its base resistors. Q_2 is also reverse biased, having its emitter at a low negative potential and its base at ground. At this stage, V_{out} is +E through R_9 and the Nixie is OFF. This state can be initiated by a positive pulse at C_3.

If it is desired that V_{out} switch from a high positive voltage to a low and negative voltage (instead of to +1 volt), then the pnp-npn flip-flop shown in Fig. 1b can be used. This is a closed R-S flip-flop. Inputs R and S are complementary logic levels and the clock is a negative pulse. In this circuit, also, both transistors are either ON or OFF. When they are ON, the collector of Q_2 is approximately at −E (less the diode drop) and this keeps Q_1 ON. Q_1's collector is then at a low negative potential (−1 volt). In this state, V_{out} is approximately −E.

When they are OFF, the base of Q_1 is at ground and its emitter is at a low negative potential (− 0.8 volt), which keeps Q_1 cut off. Q_2's base is at −E and Q_2 stays OFF. In this state, V_{out} is +E.

The purpose of D_1 in both circuits is to isolate Q_1 from Q_2 when Q_2 is OFF. In this manner, V_{out} is not loaded down.

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